Extraction of a Polynomial LDMOS Model for Distortion Simulations Using Small-Signal S-parameter Measurements

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Abstract

A method based on measured S-parameters for extracting a polynomial electro-thermal model of a 30W RF power transistor is presented. Once the package is de-embedded, the model for the intrinsic transistor can be calculated and distortion can be simulated. Simulated results match well with the measured values, revealing both thermal and electrical bandwidth dependencies of 3rd order intermodulation distortion (IM3). Component-wise Volterra analysis also shows that IM3 distortion is dominated by the nonlinearities of the input capacitance and gm in LDMOS type of transistors.

1. Introduction

Accurate distortion simulations of a power amplifier have been a challenge for the last years and Motorola's Electro-Thermal MET-model [1] for LDMOS presents current state-of-the-art in high power transistor modelling. This paper presents the measurement technique which allows the polynomial nonlinearities of individual circuit elements to be extracted. The presented polynomial model will be compared to the MET model and the measured results will be given.

Polynomial characterization technique is not widely used in transistor modelling. Probably the main reason for that is because of the integrated circuit (IC) oriented modelling research. In IC design work, very generic models that cover all the operating regimes over wide range of W/L-ratios must exist. It is evident that this kind of generic model cannot be accurate in terms of derivatives, which is the most important thing in terms of distortion simulations. Approach presented here is based on the measurements and empirical fitting of polynomial nonlinearity coefficients, which can be recalculated in every operating point. Therefore, from derivatives point of view, this empirical model is expected to be more accurate than the most of the generic models. Also, since the nonlinearities of individual circuit elements are characterized by polynomials, dominating distortion mechanisms and possible cancellation schemes can be visualized by Volterra method, which helps a lot in design optimization. It is often considered that the drawback of polynomial modelling is the limited amplitude range, in which the model is valid. This is partially true, but the linearity requirements of the modern telecommunication systems start to be so demanding nowadays, that the amplifiers have to operate in a linear region, as a result of which the truncated polynomial approach is valid.

2. Extraction procedure

Polynomial extraction technique is introduced in [2]. Pulsed S-parameters are used to avoid the effects of self-heating and extract the electro-thermal nonlinearity coefficients that contribute the distortion at low modulation frequencies. Compared to [2], high power device is now extracted, making the calibration issues more sensitive and second, the transistor includes heavy on-chip matching circuitry, which makes the de-embedding difficult. The extraction flow is presented below, and the sections of this chapter deals with these topics.

- measure the small-signal S-parameters of a packaged transistor as functions of bias voltages and temperature
- obtain the S-parameters of the package and on-chip matching network
- de-embed the s-parameters of the intrinsic FET by using a 16-term error box model for the package
- extract the small-signal circuit elements in each bias point at two temperature values
- fit a polynomial model for the measured small-signal circuit elements around the chosen bias point / along the expected load line

2.1. Pulsed S-parameter measurements

The S-parameters were measured using the test set-up presented in Fig. 1. Measurement starts when the gate voltage is triggered to set the correct bias values. After 0.5 ms, NWA measures the S-parameters of the DUT, while the oscilloscope and current probes measures the bias values. This 0.5 ms is assumed to be long enough that the electrical steady-state is obtained, but short enough that no significant amount of self-heating is introduced.

A network analyser (NWA) is calibrated through DC-blockers to the reference planes using TRL-calibration that avoids the need of accurate calibration standards. Despite of that, the calibration is very sensitive to errors, because low impedance values at high frequencies are measured. To avoid the calibration errors, accurate calibration kit similar to actual test board was build. Measurements were performed at drain and gate voltage values of 2-40 V and 3.0-4.5V at the temperatures of 0 and 75 C. The pulsed S-parameters were measured totally at 198 different operating conditions.

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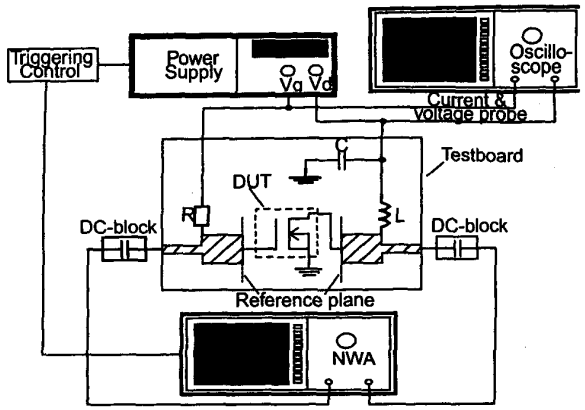

Fig. 1. Test set-up for measuring pulsed S-parameters.

2.2. The effects of the package

The S-parameters of the DUT measured in previous section include not only the intrinsic transistor, but also the extrinsic part of it. This is particularly important in MRF21030 [3] LDMOS, which is partially on-chip matched device, exhibiting a significant impedance transform. Therefore the effects of the package have to be de-embedded to gain an in-sight into the intrinsic transistor. In this work, an existing simulation model for the package of the transistor was available, so a full 16-term 4-port model for the package was simply simulated and the s-parameters of the intrinsic transistor were de-embedded using the procedure described in [4].

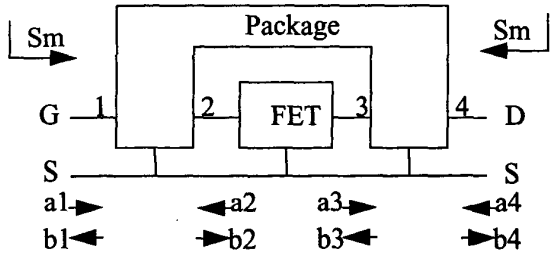

Fig. 2. Intrinsic transistor and 4-port model of the package.

2.3. Small-signal elements

The small-signal model of the LDMOS is presented in Fig. 3. It includes three capacitances Cgs, Cds and Cgd, transconductance gm and output conductance go, which are considered to be bias dependent circuit elements. Series resistances of the terminals Rg, Rd and Rs are taken as constant valued components.

The values of the circuit elements can be derived from de-empeded S-parameters, once they have been converted to Y-parameters. Since the procedures for that are well covered in the litterature [5,6], they will not be presented in this paper. Quasi-static approach described in [2] are used here, because it is valid at the measurement frequency of 2.14 GHz.

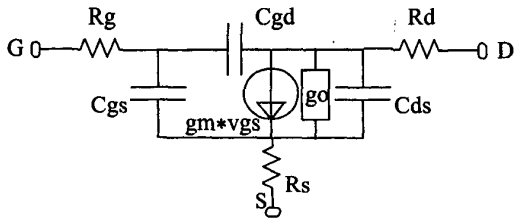

Fig. 3. Small-signal intrinsic model.

The small-signal extraction procedure based on measured and de-embedded S-parameters is applied over the range of bias voltages and temperatures. Small-signal circuit elements of MRF 21030 LDMOS are extracted at every measured 198 operation conditions. These are presented at the temperature value of 27C in Fig. 4, together with simulated small-signal elements obtained from the MET-model.

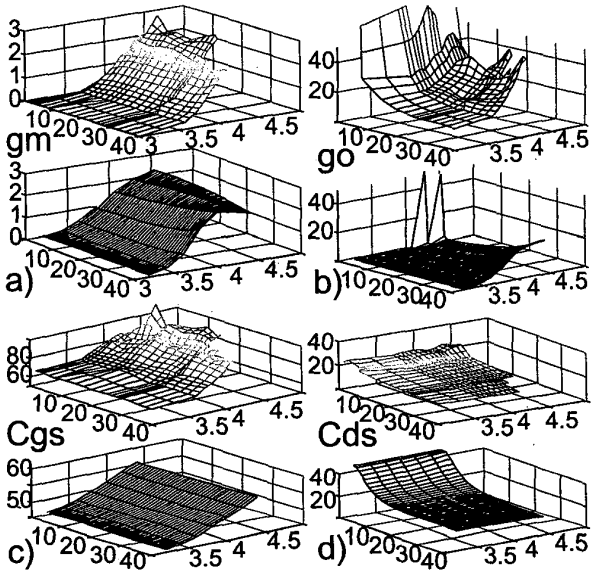

Fig. 4. A comparison between extracted and MET modelled small-signal circuit elements (x-axis Vg[V], y-axis Vd[V], z-axis gm[S],go[mS] & Cgs, Cds[pF]).

The upper surface in Fig. 4a. is measured and extracted transconductance (gm) as functions of gate and drain voltages, while the lower one is the MET-modelled gm, respectively. The two are quite similar, despite of the fact that the MET-modelled one is more linear i.e. more flat as a function of gate voltage. Fig. 4b. shows the output conductance (go), and MET modelled one is quite low and constant, while measurements show some amount of nonlinearity as functions of terminal voltages. The greatest difference between the two model are in the values of Cgs presented in Fig. 4c. The shapes are pretty much the same, but the absolute values differs about 30%. Finally, Fig. 4d show the Cds, and the only important differences are at very low drain voltage values, in which the MET modelled Cds start to increase significantly, while measured Cds increases only a little.

2.4. Fitting the polynomial model

By taking into account nonlinearities up to the third order, the drain current of an LDMOS, considered as a 3-dimensional function of gate voltage, drain voltage and temperature, can be expressed as

$$\begin{aligned} i_D &= gm \cdot v_g + K2gm \cdot v_g^2 + K3gm \cdot v_g^3 \\ &+ go \cdot v_d + K2go \cdot v_d^2 + K3go \cdot v_d^3 \\ &+ K2gmgo \cdot v_g \cdot v_d + K3gm2go \cdot v_g^2 \cdot v_d \\ &+ K3gmgo2 \cdot v_g \cdot v_d^2 + K3Tgm \cdot T \cdot v_g \\ &+ K3Tgo \cdot T \cdot v_d + K2T \cdot T \end{aligned} \quad (1)$$

The first terms in rows 1 and 2 represent small-signal transconductance and output conductance. The next two terms stand for nonlinearity, and the following three, referred to as cross-terms, represent the interaction between gate and drain voltages. Since temperature is considered an independent variable, the last three terms are required for the characterization of temperature-related effects. Dynamic temperature variations occur up to the modulation band (not at the RF band), and therefore in Eq. (1) the temperature can be considered as a 2nd order effect as explained in [7]. Only the current equation is presented in here, but similar equations for nonlinear capacitances are used, which are considered as 2-dimensional functions of voltage and temperature.

Detailed description of calculation of nonlinearity coefficients based on small signal elements is given in [2] and only a results of MRF21030 nonlinearities will be presented here. In Fig. 5, the first column corresponds to the first, second and third order nonlinearity in the transconductance exhibiting normalized nonlinearity coefficient values around one, while the second column shows the nonlinearity in the output conductance that was found to be quite linear.

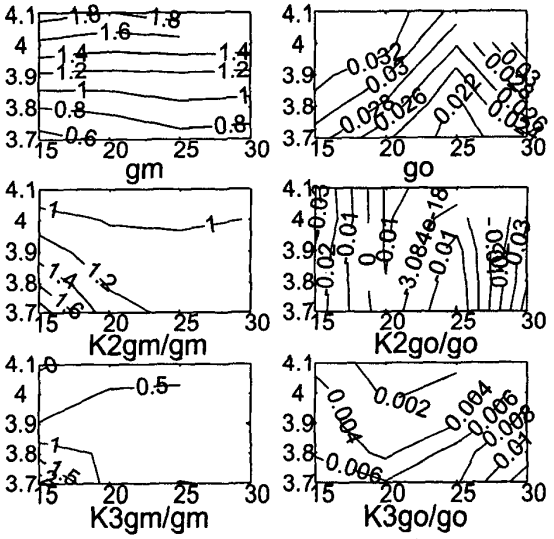

Fig. 5. Transconductance and output conductance (vertical Vg [V], horizontal Vd [V]).

Columns 1 and 2 in Fig. 6. give the cross-terms and electro-thermal terms. K2T is purely temperature dependent, while K3Tgm and K3Tgo are the combined effects of temperature and terminal voltages.

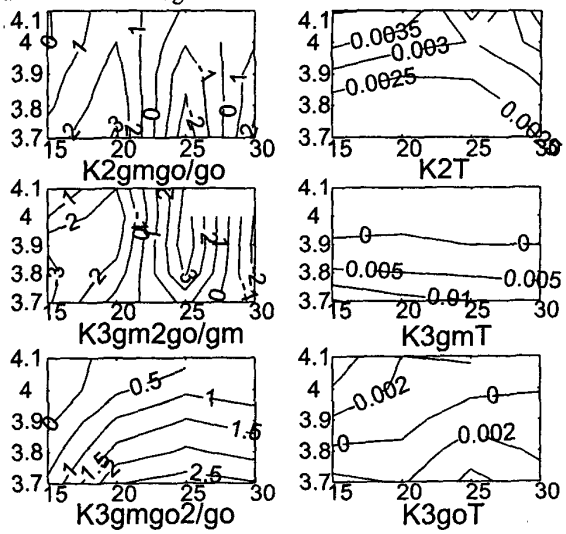

Fig. 6. Cross-terms and electro-thermal terms (vertical Vg [V], horizontal Vd [V]).

Cgs is also considered as a nonlinear, 2-dimensional function of gate-to-source voltage and temperature. Fig. 7 shows the nonlinearity coefficients with respect to these two factors. In addition, Cds and Cdg are also slightly nonlinear, but since their effects to the distortion are small, these nonlinearities are not presented here. However, the absolute values are presented in Fig. 7.

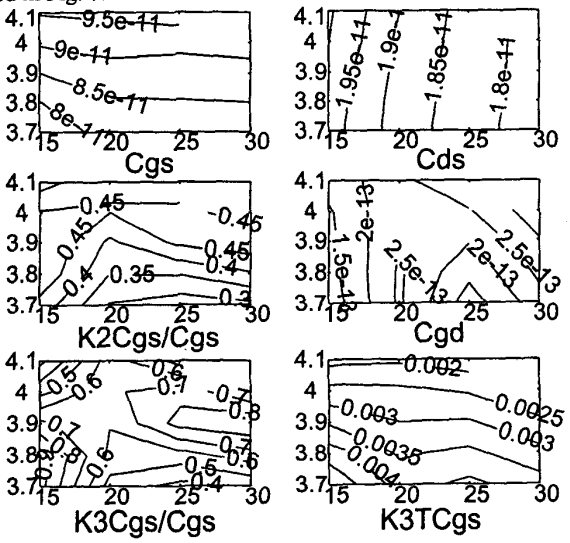

Fig. 7. Nonlinearity of Cgs, and absolute values of Cds and Cgd (vertical Vg [V], horizontal Vd [V]).

3. Linearity simulations

Next the extracted polynomial LDMOS model is simulated using the Volterra series. Another approach would be the use of numerical harmonic balance (HB) simulator, but Volterra approach shows the IM3 as a vector sum of its contributors, giving in-sigth into the dominating distortion mechanisms and possible cancellation schemes to optimize the matching impedances and bias voltages.

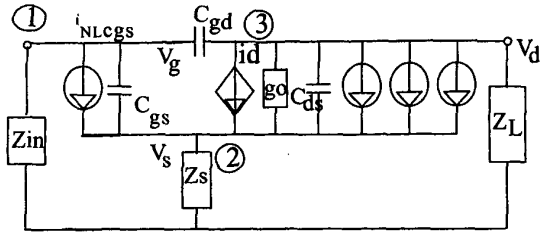

Fig. 8. A circuit containing 2nd order distortion sources. The thermal ones can be obtained by connecting inl2cgsT in parallel to inl2cg and inl2gmT to inl2gm.

Circuit to be solved for 2nd order responses is given in Fig. 8. Terminal impedances Zin, ZL and Zs includes the impedances of the package discussed in section 2.2 and out-of-chip terminal impedances were measured from actual amplifier designed according to the data sheet. Nonlinearities of the individual circuit elements are modelled by current sources using the direct method explained in [8]. Equations for third order intermodulation products (IM3) are derived in [9] and only simulation results will be given here.

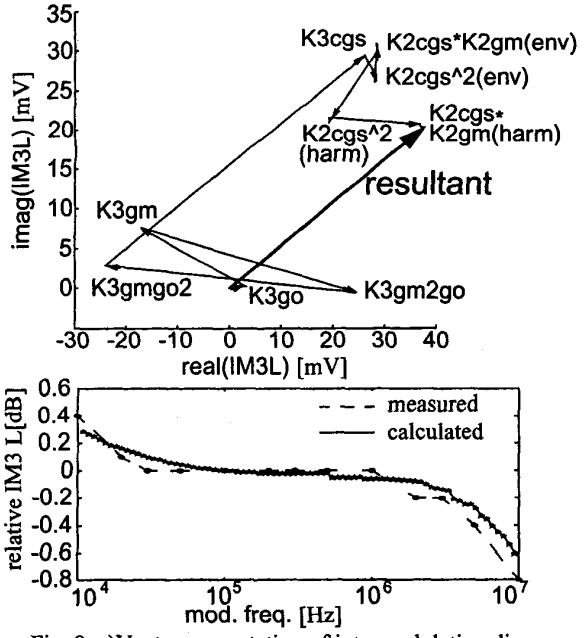

Fig. 9. a)Vector presentation of intermodulation distortion and b) amplitude of IM3 as a function of the tone difference.

Vector representation of IM3L at the 2-tone test at 2.14 GHz +/- 1MHz is presented in Fig. 9a. Distortion of the amplifier are being dominated by the nonlinearity of the tranconductance, input capacitance Cgs and mixing between these two. The nonlinearity of Cds and Cgd are negligible, and since the absolute value of Cgd is small, no significant amount of distortion feedback exists. This is proven by negligible amount of K2gm^2,harm (K2gm itself is significant), which requires the 2nd harmonic is fed back to the gate through Cdg.

The tone difference sweep is simulated and compared to the measurements in Fig. 9b, which presents relative absolute values of IM3L. Approximately 1dB variations over a modulation band of 10 MHz are observed, and Volterra simulations agree very well with the measurements. Low frequency variations are caused by dynamic temperature variations on the chip (Zth roughly estimated from Rth), while high frequency behaviour is caused by K2Cgs. These variations are usually called as memory effects considered more detail in [7].

4. Summary

Polynomial extraction technique can be successfully applied for partially on-chip matched high power LDMOS transistors, if the model of the package exists. Method based on the small-signal S-parameter measurements yields intrinsic circuit element values, whose nonlinearities are calculated based on the voltage and temperature dependencies of the elements. The measured and extracted circuit elements differ from the ones obtained from the MET model. The polynomially calculated IM3 vs. signal bandwidth match well with measured data.

References

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